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1. Your reference	534GB
2. Patent application number *(The Patent Office will fill in this part)*	**0200575.9**
3. Full name, address and postcode of the or of each applicant *(underline all surnames)*	RLS merilna tehnika d.o.o. C.11 Grupe Odredov 25 1261 Ljubljana-Dobrunje Slovenia
Patents ADP number *(if you know it)*	8302721001
If the applicant is a corporate body, give the country/state of its incorporation	Slovenia
4. Title of the invention	Encoder With Reference Marks
5. Name of your agent *(if you have one)*	J T Jackson et al
"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	Renishaw plc Patent Department New Mills Wotton-under-Edge Gloucestershire GL12 8JR
Patents ADP number *(if you know it)*	2691003

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
	-	-	-

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application	Date of filing *(day / month / year)*
	-	-

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body.* *See note (d))*	Yes

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Continuation sheets of this form	0
Description	10
Claim *(s)*	0
Abstract	0
Drawing *(s)*	1+1

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10. If you are also filing any of the following, state how many against each item.

Priority documents	0
Translations of priority documents	0
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	0
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Request for substantive examination *(Patents Form 10/77)*	0
Any other documents *(please specify)*	0

11. I/We request the grant of a patent on the basis of this application.

Signature Date 10/01/2002

AGENT FOR THE APPLICANT

12. Name and daytime telephone number of person to contact in the United Kingdom: A ILES 01453 524524

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ENCODER WITH REFERENCE MARKS

This invention relates to encoders.

Known incremental encoders comprise a scale with regular incremental marks, and a scale reader which is movable along the scale, producing output pulses or cyclic waveforms in response to the incremental marks as they pass. The output is taken to a counter which counts the incremental pulses or cycles thus produced, making it possible to measure the distance travelled.

It is known to provide the incremental marks in one track along a scale, and to provide a parallel track which contains one or more reference marks. The readhead has a suitable detector for detecting the reference mark. By resetting the counter when the reference mark is detected, it is possible for the counter output to indicate an absolute position, i.e. the actual distance from the position of the reference mark.

Where there are several reference marks in the reference track, it is desirable for the user to be able to select which of the reference marks to use, i.e. which one is to reset the counter.

The present invention provides an encoder comprising a scale and a scale reader;

the scale having a series of incremental marks extending along its length, and a plurality of reference marks spaced apart in the lengthways direction;

the scale reader including means for reading the

incremental marks and producing an output therefrom, and for reading the reference marks;

characterised in that:

the reference marks are arranged along the scale in a random or pseudo-random pattern;

as the scale reader moves over the pattern of the reference marks, it continually compares the pattern with a previously stored pattern; and

when the pattern of the reference marks matches the previously stored pattern, it outputs a reference signal.

In a preferred embodiment, the scale reader reads the pattern of the reference marks into a shift register as it passes over them, and the pattern in the shift register is compared to the previously stored pattern. Values may be introduced into one end of the shift register, depending upon the values received from the pattern of the reference marks, and these values may be shifted along the shift register synchronously with the passing of the scale reader over the reference marks. Preferably values may be introduced into either end of the shift register, depending upon the direction of travel of the scale reader along the scale.

A preferred embodiment of the invention will now be described by way of example, with reference to the accompanying drawings, wherein:

Fig 1 is a schematic diagram showing a scale, a readhead and circuitry for producing a reference signal.

Fig 1 shows an elongate scale 10, along which a scale reader 12 can run. In practice, the scale 10 and scale

reader 12 are fixed to respective relatively movable members of a machine, and measure their relative movement.

The scale 10 includes an incremental track 10a, comprising a series of spaced marks which are read by a readhead 1 in the scale reader 12. In the preferred embodiment, the marks of the incremental track are magnetic marks, spaced for example 1mm apart, and the readhead 1 is an integrated circuit chip designated POT sold by the present applicants RLS d.o.o., Slovenia.

This chip produces raw sine and cosine outputs (sin1, cos1) from the scale marks. From these it generates quadrature squarewaves on lines A,B, which by interpolation within the chip can be generated at 25 times the pitch of the incremental track 10a. It also generates a reference pulse Ri1 every period of the incremental track, when sin1 equals cos1, and sin1 and cos1 are both greater that zero. This reference pulse has a width corresponding to 10μm.

An additional clock pulse CLK is derived every period of the incremental track from the outputs sin1, cos1 of the readhead chip 1, by comparators 50 and an AND gate 52.

The POT chip incorporates Hall effect sensors to react to the magnetic scale marks. The technology for producing the signals sin1, cos1, A, B and Ri1 is well-known and will not be described further. Of course, scales with other pitches could be used. Other magnetic readheads could be used instead of the POT chips. The invention is also applicable to scales

using technology other than magnetic, e.g. optical scales and opto-electronic scale readers.

The quadrature incremental signals A,B provide the output of the device, and are taken to an up-down counter (not shown) in the normal way in order to count the position of the scale reader 12 along the scale 10.

The scale 10 also includes a coded reference track 10b, alongside the incremental track 10a. As shown, this may be produced simply by extending selected ones of the incremental marks sideways. However, it is possible to provide a separate reference track instead. It is also possible to provide two reference tracks, arranged symmetrically on either side of the incremental track 10a, so that the scale can be fitted either way round in practice.

The magnetic marks in the reference track 10b form a pseudo-random code, chosen such that the code only repeats at certain intervals. In a simple 4-bit example, the following code pattern may be used repeatedly:

....0 0 0 0 1 0 0 1 1 0 1 0 1 1 1 1 0 0 0....

(where 1 and 0 represent the presence and absence of a mark).

Each successive 4-bit pattern in this code provides a unique value. There are sixteen different values, which repeat every 16mm if the period of the scale is 1mm, as follows:

0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	1
0	0	1	1
0	1	1	0
1	1	0	1
1	0	1	0
0	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1
1	1	1	0
1	1	0	0
1	0	0	0
0	0	0	0

In practice, it will often be preferable to use a longer pseudo-random code, for example an 8-bit code. A suitable code pattern for an 8-bit code which repeats only every 256mm is as follows:

... 0 1 0 0 0 0 0 0 1 1 0 0 0 0 0 1 0 1 0 0 0 0 0 1 1 1
0 0 0 0 1 0 0 1 0 0 0 0 1 0 1 1 0 0 0 0 1 1 0 1 0 0 0 0
1 1 1 1 0 0 0 1 0 0 0 1 0 0 1 1 0 0 0 1 0 1 0 1 0 0 0 1
0 1 1 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 1 1 0 0 0 1 1 1 0 1
0 0 0 1 1 1 1 1 0 0 1 0 0 1 0 1 0 0 1 0 0 1 1 1 0 0 1 0
1 0 1 1 0 0 1 0 1 1 0 1 0 0 1 0 1 1 1 1 0 0 1 1 0 0 1 1
0 1 0 1 0 0 1 1 0 1 1 1 0 0 1 1 1 0 1 1 0 0 1 1 1 1 0 1
0 0 1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 0 1 0 1 1 0 1 1 0 1
0 1 1 1 1 1 0 1 1 0 1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1 0
0 0 0 0 0 0 ...

In this code sequence, each successive 8-bit pattern provides a unique value. The first few of these values are as follows:

0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	1
0	0	0	0	0	0	1	1
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	0
0	0	0	1	1	0	0	0
etc.							

Even longer codes could be used if greater repeat intervals were needed, e.g. 14 or 15-bit codes. With a greater repeat interval, the user can have a longer length of scale within which it is possible to select a unique code value for the reference.

The coded reference track 10b is read by two readheads 2,3 within the scale reader 12. For economy, these may be POT chips which are identical with the readhead 1, although this is not essential. A single readhead for the reference track would also be possible, though the reason we prefer to use two will become apparent shortly. The position of readhead chip 1 relative to readhead chips 2 and 3 should be such that the clock signal CLK appears at the time when readhead chips 2 and 3 are sensing the presence of a magnetic mark in the reference track 10b.

Analogue outputs from the POT chips 2,3 are used. These may be the sine or cosine signals, or a reference signal derived from them. The outputs from the chips 2,3 are taken to comparators 14,16, where they are squared up. Thus, each comparator 14,16 provides a digital pulse train, which may be represented as a train of 0s and 1s, corresponding to the code of the marks in the reference track 10b.

As seen in Fig 1, the pulse trains from the comparators 14,16 are fed to data inputs DSR,DSL at opposite ends of a bi-directional shift register 18. The shift register 18 has as many bits as the number of bits of the pseudo-random code, e.g. 4 bits or 8 bits in the above examples. The shift register 18 is clocked at an input CLK by the reference pulses from the comparators 50 and AND gate 52. Thus, one new data bit is read into one or other end of the shift register for each period of the scale 10, and this data bit will correspond to an 0 or 1 of the pseudo-random code of the reference track 10b.

A direction detector 20 receives the quadrature outputs A,B of the readhead 1, and produces an output which is high or low, depending on the direction of travel of the scale reader 12 along the scale 10. This is taken to a direction input SL and (via an inverter 22) to a complementary direction input SR of the shift register 18, in order to determine the direction in which the data bits are shifted through the shift register. Thus, when the scale reader moves towards the right (as seen in Fig 1) new data values from the pseudo-random code in the reference track 10b are picked up by the readhead 3 and fed into the shift register 18 from right to left via the input DSL. Conversely, when the scale reader 12 is moving towards the left, new values of the pseudo-random code are fed into the shift register from left to right via the input DSR.

The readheads 2,3 of the scale reader 12 are deliberately spaced apart by a distance corresponding to one word of the pseudo-random code. Thus, for example, in the case of a 4-bit code, and a 1mm period

scale, the readheads 2,3 are spaced apart by 4mm. In the case of an 8-bit code, and a 1mm period, they are spaced by 8mm.

It will be seen that as a result, the bits held in the shift register 18 always correspond to the code bits which are in the reference track 10b between the readheads 2,3, and are continually maintained up to date as the scale reader 12 moves along the scale 10.

The readhead 1 is preferably spaced mid-way between the readheads 2,3 in the scale reader 12. However, this is not essential, as long as the phase of the clock pulse CLK is correct, compared to the readheads 2 and 3, so that the pulses from the code track are correctly sampled by the shift register 18.

When the scale 10 and scale reader 12 are installed on a machine, one particular value of the pseudo-random code will be chosen as a reference value, and as described below is stored in a memory 24. The memory 24 may for example consist of an electrically erasable and programmable read-only memory (EEPROM). A comparator 26 continually compares the outputs of the shift register 18 with the output of the memory 24. When the scale reader 12 is moved into a position relative to the scale 10 such that the value in the shift register 18 is equal to the value in the memory 24, the comparator 26 provides an output to an AND gate 28. Here, it is ANDed with the 10μm reference pulse Ri1, producing a 10μm output Ri. This may be taken to the control system of the machine upon which the scale and scale reader are installed, as a reference pulse, for example in order to reset the counter which counts

the quadrature signals A,B from the incremental track 10a. The counter can thus be reset should it have lost count for any reason, e.g. when the system is first switched on or if there is a power outage.

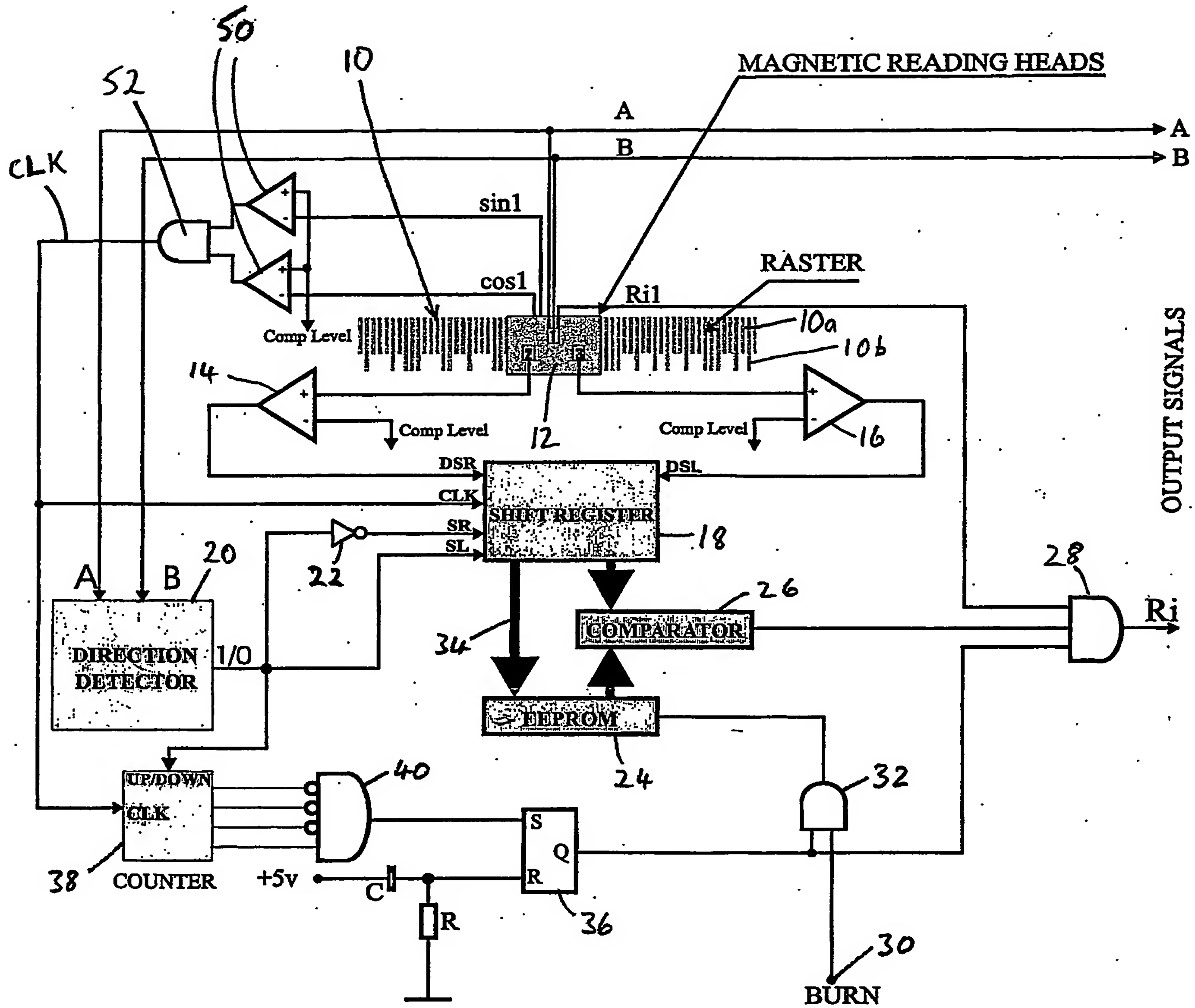
The manner in which a selected code value is stored in the memory 24 will now be described. The scale reader 12 is moved to a desired position on the scale 10, and an input is then provided to a "burn" input 30, e.g. from a push-button. This is taken via an AND gate 32 to the memory 24, and causes the current value from the shift register 18 to be burnt into the memory 24 via a bus 34.

However, it will be appreciated that if the system has just been switched on, the data in the shift register 18 will not be valid. The scale reader 12 must move by at least the length of the code (e.g. 8mm in the case of an 8-bit code and a 1mm scale period) in order for the data to be valid. This condition is indicated by the output of a flip-flop 36, which is reset upon power-up by a capacitor-resistor circuit C,R. In this condition, it inhibits both the AND gate 32 (to prevent invalid data being burnt into the memory 24) and also the AND gate 28 (to prevent an invalid output reference pulse Ri).

The flip-flop 36 is set, enabling the AND gates 32,28, when a counter 38 and gate 40 indicate that the scale reader 12 has moved by a sufficient distance. They do this by counting the clock pulses CLK from the readhead 1.

In a simpler system, the memory 24 could be a DIP

switch, having as many as switches as there are bits of the pseudo-random code. The code value at which the reference pulse Ri is to be generated is then set manually on these switches.



MAGNETIC READING HEADS
50
52
10
CLK
A
B
sin1
cos1
Ri1
RASTER
Comp Level
10a
10b
14
Comp Level
12
Comp Level
16
DSR
DSL
CLK
SHIFT REGISTER
SR
SL
18
20
22
A
B
DIRECTION DETECTOR
1/0
34
26
COMPARATOR
28
Ri
EEPROM
24
UP/DOWN
CLK
COUNTER
38
40
+5v
C
R
S
Q
R
36
32
30
BURN
OUTPUT SIGNALS

FIG 1